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DESIGN FOR PACKAGEABILITY

Early Consideration of Packaging

from a Microelectronic System Designer's Viewpoint

DARPA Order A879

DHHS A-04-94-04532

AMXRO-AAA: P-32575-EL

FINAL REPORT for 1 Jan 94 - 31 Dec 97

by

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EXECUTIVE SUMMARY

The goal of this project was to assist in globally optimizing the design of higher performing microelectronic systems by incorporating critical packaging factors into the IC design flow. More specifically, our work was intended to empower system designers, especially designers of multi-million transistor ICs, to obtain optimized MCM-based systems.

This work is innovative with respect to the following:

- The concept of Design for Packageability had not been fully developed nor documented.
- The procedure for using area-array pads rather than peripheral pads had not been documented and promulgated publicly.
- A comprehensive system model that can be used to analyze and compare from a system designer's viewpoint the impact of different packaging technologies and different IC design methodologies did not exist.
- Early analysis CAD software incorporating such a system model was not available.
- Commercial CAD software for designing ICs did not include consideration of critical packaging parameters.
- MCM prototyping via a multi-project broker had not been conducted by university designers.

Multi-chip integration technology has the potential to increase significantly overall system performance and reliability while reducing size, weight, power and cost. The work conducted for this project explored and demonstrated the impact of these MCM-based technologies on IC design and, hence, on the overall system. Development and verification of the Design for Packageability procedures was performed to accelerate the architectural exploitation of both ICs and MCMs.

Thus, the major accomplishments of this effort are:

- **Early Analysis and Design Space Exploration Tools**

  We developed a set of CAD tools which permit exploration of the IC and packaging design space simultaneously. This approach emphasizes concurrent consideration of the partitioning of a microelectronic circuit design into multiple dies and the selection of the appropriate packaging technology for implementation of the entire system. Partitioning a large design into a multichip package is a non-trivial task. Similarly, selection of the MCM packaging technology to accommodate a multichip solution can also be puzzling. The interdependencies of these two problems afford the opportunity to achieve a global optimum when considered concurrently. In our tool we address the partitioning/MCM technology tradeoff and their interdependency. The SUN MicroSparc CPU was used as a demonstration vehicle and was partitioned for different MCM technologies. The results show that the optimum number of partitions and contents of each partition depend heavily on the choice of MCM technologies for a given application.

- **Area-array pad router**

  Arranging I/O in a matrix array over the core circuitry of an IC generally provides 5- 10 times more I/O than the traditional method of restricting pads to the periphery. This approach also minimizes overall die size. This method was pioneered by IBM over thirty years ago and has recently become attractive for new designs requiring several hundred I/O. In this project we developed a new area-array pad router which differs from other approaches in that no additional metal layer is added (unless needed) and no redistribution is required. We developed a design guideline definition, data preparation, pad placement, pad assignment, pad routing, and output padframe generation for this technique. The new router was used to provide for area-array I/O on the partitioned MCM dies requiring 112, 298 and 485 I/Os.

- **MCM Prototyping Via MIDAS**

  Our project was the one of the first to exercise the new multi-project prototyping service introduced by MIDAS. We designed a general-purpose programmable DSP subsystem that was packaged in a multichip module. The subsystem contained a 32-bit floating-point programmable DSP processor along with 256 K-bytes of SRAM, 128 K-bytes of EEPROM, a 10 K-gate FPGA and a 6-channel 12-bit ADC. The complete subsystem was interconnected on a 37 mm by 37 mm MCM-D substrate and packaged in a 320-pin ceramic quad flat pack. The design was submitted to the MIDAS brokerage service and fabricated by Micro Module Systems. Our experience showed that low-volume MCM prototyping is achievable and somewhat affordable for universities. The design flow, electrical and thermal analyses, CAD tools, cost and lessons learned were documented.

IMPACT AND TECHNOLOGY TRANSFER

This research project has made significant impact on this emerging field in the following ways:

1. Our early analysis approach which permits MCM-based system optimization by incorporating critical packaging factors into the design of the integrated circuits is now being adopted by other designers. Specifically, the the title and scope of the IEEE Multi-Chip Module Conference which has been held annually in Santa Cruz, CA, for the past seven years was changed in 1998 to IEEE Symposium on IC/Package Design Integration. Several papers from industry and academia were presented using the approach which we pioneered.

2. The early analysis tools that we developed are available for others to use. Following a presentation we made at Georgia Tech, Prof. Sudha Yalamanchili visited us and has since adopted our approach.

3. The area-array pad router for ICs is now available for others to use. Our work stimulated and complemented the development of a similar commercial tool developed by Cascade Design Automation.

4. Our pioneering the design and prototyping of a MCM via the MIDAS brokerage has enabled MIDAS to adopt regularly scheduled fabrication runs. Our experiences resulted in the principal graduate student designer winning the First Place Award in an international contest sponsored by the Mentor Graphics Corporation. Furthermore, the procedure for MCM design and prototyping is being used in a graduate course at the University of Tennessee to serve as a model for other universities to follow.

5. Dr. Peyman Dehkordi, one of the principal contributors to this DARPA project, has launched a commercial spin-off company to assist industry and government agencies in exploiting the fruits of this research. The company, called Applied Computing Technologies, is located in nearby Oak Ridge, TN. It anticipates designing a MCM for the Air Force Research Lab in Albuquerque as part of

their Highly Integrated Packaging and Processing program. Furthermore, a new commercial MCM product is being developed by the company.

6. Another form of technology transfer is the production of newly trained graduates who can help industry in a variety of ways. Individuals who were involved in this research project and their current employers include:

Researcher	**Employer**
Chattapadhyay, Subho	Motorola, Austin, TX
Dehkordi, Peyman	ACT, Oak Ridge, TN
Devine, Quinn	Intel, Phoenix, AZ
Ghazi, Sassine	Intel, Phoenix, AZ
Govindan, Rajeev	QualComm, San Diego, CA
Neiroukh, Osama	Intel, Hillsboro, OR
Powell, Tim	Cadence, Cary, NC
Ramamurthi, Karthi	Intel, Sacramento, CA
Shen, Zijun	Analog Devices, Greenboro, NC
Tan, Chandra	Univ. of Tennessee, Knoxville, TN
Tolnas, Barry	Intel, DuPont, WA
Williams, Nicolas	Tanner EDA, Pasadena, CA
York, John	Lockheed 3-D, Orlando, FL

APPENDICIES

The following publications and presentations document in detail the work conducted for this project. Since these papers were peer-reviewed, their acceptance by the community certifies the significance and quality of our efforts.

1. Bouldin, D., "Design for Packageability", Presentation at DARPA Principal Investigators' Meeting, May 1997.

2. Dehkordi, P., Ramamurthi, K., Bouldin, D., Davidson, H., and P. Sandborn, "Impact of MCM Technology on Microelectronic Systems Partitioning: A Case Study", *Proceedings of 1995 IEEE Multi-Chip Module Conference*, Santa Cruz, CA, February 1-2, 1995.

3. Bouldin, D. and P. Dehkordi, "Design for Packageability: An Overview", *Proceedings of 1995 International Intersociety Electronic Packaging Conference*, Lahaina, HI, March 26-30, 1995.

4. Chattapadhyay, S., Dehkordi, P., and D. Bouldin, "An Overview of Placement and Routing Algorithms for Multi-Chip Modules", *International Journal of High Speed Electronics - Special Issue on CAD for Multichip Modules*, December, 1995.

5. Dehkordi, P., Powell, T., and D. Bouldin, "Development of a DSP/MCM Subsystem: Assessing Low-Volume, Low-Cost MCM Prototyping for Universities", *Proceedings of 1996 IEEE Multi-Chip Module Conference*, Santa Cruz, CA, February 5-7, 1996.

6. Dehkordi, P., Ramamurthi, K., Bouldin, D., and H. Davidson, "Early Cost/Performance Cache Analysis of a Split MCM-Based MicroSparc CPU", *Proceedings of 1996 IEEE Multi-Chip Module Conference*, Santa Cruz, CA, February 5-7, 1996.

7. Dehkordi, P., Powell, T., and D. Bouldin, "Performance Comparison of MCM-D and SMT Packaging Technologies for a DSP Subsystem", *Proceedings of 1996*

IEEE International Symposium on Circuits and Systems Conference, pp. IV-245 thru IV-248, Atlanta, GA, May 12-15, 1996.

8. Dehkordi, P., Chandra, T. and D. Bouldin, "Intrinsic Area Array ICs: What, Why, and How", *Proceedings of 1997 IEEE Multi-Chip Module Conference*, Santa Cruz, CA, February 4-5, 1997.

9. Dehkordi, P., Ramamurthi, K., Bouldin, D. and H. Davidson, "Determination of Optimum Area-Array Bond Pitch for MCM Systems", *Proceedings of 1997 IEEE Multi-Chip Module Conference*, Santa Cruz, CA, February 4-5, 1997.

10. Tan, C., Bouldin, D. and P. Dehkordi, "An Intrinsic Area-Array Pad Router for ICs", *Proceedings of Tenth Annual IEEE International ASIC Conference*, pp. 265-269, Portland, OR, September 7-10, 1997.

11. Tan, C., Bouldin, D. and P. Dehkordi, "Design Implementation of Intrinsic Area Array ICs", *Proceedings of 1997 Advanced Research in Very Large Scale Integration Conference*, Ann Arbor, MI, September 15-16, 1997.

12. York, J., Powell, T., Dehkordi, P. and D. Bouldin, "Enhancement of MCM Testability Using an Embedded Reconfigurable FPGA", *Proceedings of 1997 International Conference on Innovative Systems in Silicon*, pp. 165-173, Austin, TX, October 8-10, 1997.